

CLAIMS:

What is claimed is:

- 1 1. A partly reprogrammable Finite State Machine including  
2 a state register holding the current state and two functions (of  
3 and *nf*) comprising combinational logic to calculate the outputs  
4 and the next state, respectively, said combinational functions  
5 being representable in a "sum of product terms form", said  
6 Finite State Machine comprising:
  - 7 a) a circuit disabling a predetermined number of product  
8 terms associated with said "sum of product terms form", each  
9 product term corresponding to a given state and a given input  
10 vector setting,
  - 11 b) a circuit enabling a new product term for a predetermined  
12 respective number of new product terms generating for each, a  
13 correct output signal corresponding to a given error state and a  
14 given error input bit vector, and
  - 15 c) said disabling and /or enabling circuits being provided  
16 in a form which allows activation thereof in case a product term  
17 was tested to include a bug.
- 1 2. The state machine according to claim 1, in which the  
2 circuit disabling a predetermined number of product terms  
3 comprises a control latch, the output of which connects to a  
4 logical AND gate, the input signals of which further comprise  
5 signal lines associated with the error state and the respective  
6 input vector.

1     3.       The state machine according to claim 1, in which the  
2     circuit disabling a predetermined number of product terms  
3     comprises a respective number of disable registers, each  
4     associated with a respective decoder.

1     4.       The state machine according to claim 1, in which the  
2     circuit enabling a new product term comprises:  
3         a) an input mask register,  
4         b) an input compare register,  
5         c) a state compare register, and  
6         d) an output register, which holds the corrected output  
7     signals.

1     5.       The state machine according to claim 4 which further  
2     comprises a next state register, which holds the output signals  
3     for the next state.

1     6.       The state machine according to claim 1, further  
2     comprising:  
3         a) circuit disabling an error-comprising otherwise logic,  
4     and  
5         b) circuit enabling a new corrected otherwise logic,  
6     which comprises logic reflecting enabled new product terms.

1     7.       The state machine according to claim 1 in which,  
2         the circuit disabling a predetermined number of product  
3     terms, the circuit enabling a predetermined respective number of  
4     new product terms and a corrected output signal vector are  
5     programmed in a content addressable memory, and  
6         whereby the error state and the error input vector is  
7     used as a search argument into said content addressable memory.

1     8.       The state machine according to claim 1 in which the  
2     circuit enabling a new product term comprises a Random Access  
3     Memory (RAM) including logic creating a corrected output vector,  
4     and a RAM address generation logic is provided for selectively  
5     accessing respective RAM entries, and a state machine select  
6     logic is provided for selecting between activation of either the  
7     regular state machine or the RAM for generating a desired output  
8     vector.

1     9.       The state machine according to claim 8 in which the RAM  
2     comprises a plurality of compartments, each of them comprising  
3     input mask logic, input compare logic, next state logic and  
4     correct product term output signal logic, respectively.